REMARKS

Claims 1-30 are pending in this application. By this Amendment, independent claims 1, 8, 19 and 28 are amended for clarity, while claims 7, 14, 20 and 29 are amended to correct informalities. Support for the amendments to the independent claims can be found, for example, at least at page 8, lines 1-8 and lines 22-24, at page 9, lines 6-8, at page 9, line 29 through page 10, line 1, at page 10, lines 8-26, and in Figs. 4 and 5. No new matter is added.

The courtesies extended to Applicant's representatives by Examiner Bengzon at the personal interview held January 10, 2008, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below, which constitute Applicant's record of the interview.

The Office Action rejects claims 1-11, 14-18 and 28-30 under 35 U.S.C. §103(a) over Narasimhan (U.S. Patent No. 6,446,192) in view of Bishop (U.S. Patent No. 4,914,653) and rejects claims 12, 13 and 19-27 under 35 U.S.C. §103(a) over Narasimhan in view of Bishop, and further in view of Balachandran (U.S. Publication No. 2005/0078620). The rejections are respectfully traversed.

Specifically, Applicant respectfully asserts that Narasimhan fails to disclose or suggest, either alone or in combination, the combination of features recited in independent claims 1, 8, 15, 19 and 28. Among other features, Narasimhan fails to disclose or suggest a management part having at least a management block to receive command data through a predetermined logic channel in the inbound link and generate a corresponding command signal on the microprocessor bus system to perform a management function for the microprocessor system, the management block being further adapted to receive a response signal from the microprocessor bus system and

transmit corresponding response data through a predetermined logic channel in the outbound link, as recited by independent claim 1.

Narasimhan merely discloses a network interface chip (NIC) that is used to connect a device to a standard network, such as a TCP/IP connection. See col. 2, lines 41-54 and col. 3, lines 16-24. As can be clearly seen in Fig. 9, Narasimhan teaches an NIC to provide an interface between a standard network (32) and a system bus (50), the device bus providing communication between a microprocessor (52) and peripherals such as external memory (54). This interface is further described in at col. 7, lines 21-36, and displayed in Fig. 2. Narasimhan discloses that the two primary connections to the NIC are the device interface connections and the network interface connections, which connect to the physical interface circuitry of the network. Thus, Narasimhan discloses communication between the network and the device interface connections.

The device interface are connections connected to the NIC through an system bus. The NIC appears to the processor as simply another slave peripheral device. See Narasimhan, col. 14, lines 24-26. Thus, the processor communicates to the NIC over a system bus through the processor's communication port using the appropriate protocol for the system inter-processor bus and does not communicate directly over the micropocessor bus system that provides a communication path between the processor core and at least one processor subsyem, as recited by independent claim 1. Accordingly, Narasimhan neither discloses nor suggests any connection to the bus internal to the microprocessor which is connected to the processor core, and therefore showing that the disclosed NIC of Narasimhan is incapable of generating command signals on the microprocessor bus. Thus, Narasimhan clearly fails to disclose or suggest a management block that generates a corresponding command signal on the microprocessor bus system to perform a management function for the microprocessor system, as recited by independent claim

1. Independent claims 8, 15, 19 and 28 similarly recite these features. Thus, independent claims 1, 8, 15, 19 and 28 are patentable over Narasimhan.

Bishop fails to overcome the deficiencies of Narasimhan. Bishop is relied upon to disclose inter-processor communication over logic channels. However, Bishop also fails to disclose or suggest a management block that generates a corresponding command signal on the microprocessor bus system to perform a management function for the microprocessor system, as recited by independent claims 1, 8, 15, 19 and 28.

Still further, Balachandran fails to cure the deficiencies of Narasimhan and Bishop, and therefore, independent claims 1, 8, 15, 19 and 28, and their dependent claims are patentable over Narasimhan, Bishop and Balachandran, whether considered in combination or separately. Accordingly, withdrawal of the rejections is requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of all pending claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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